

MODEL NAME : *PLW00*

PCB NO : *LA-7452P*

BOM P/N : *TBD*
TBD

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Schematic Document

Breitling (Huron River)

Sandy Bridge (BGA) + Cougar Point (standard)

DISCRETE VGA N12P-GV-S-A1 (optimus)

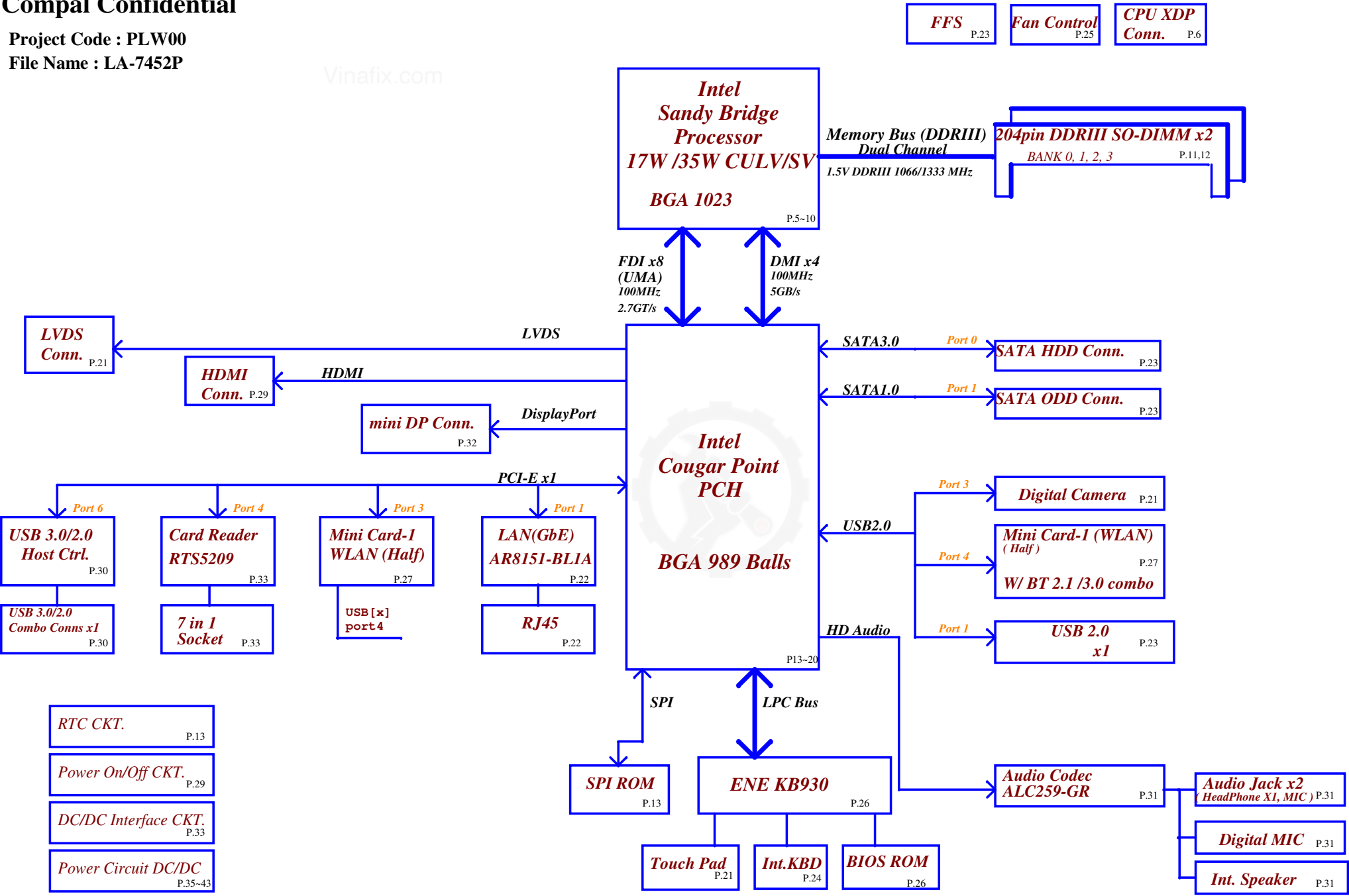
2011-07-12

Rev: 1.0

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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	Cover Page
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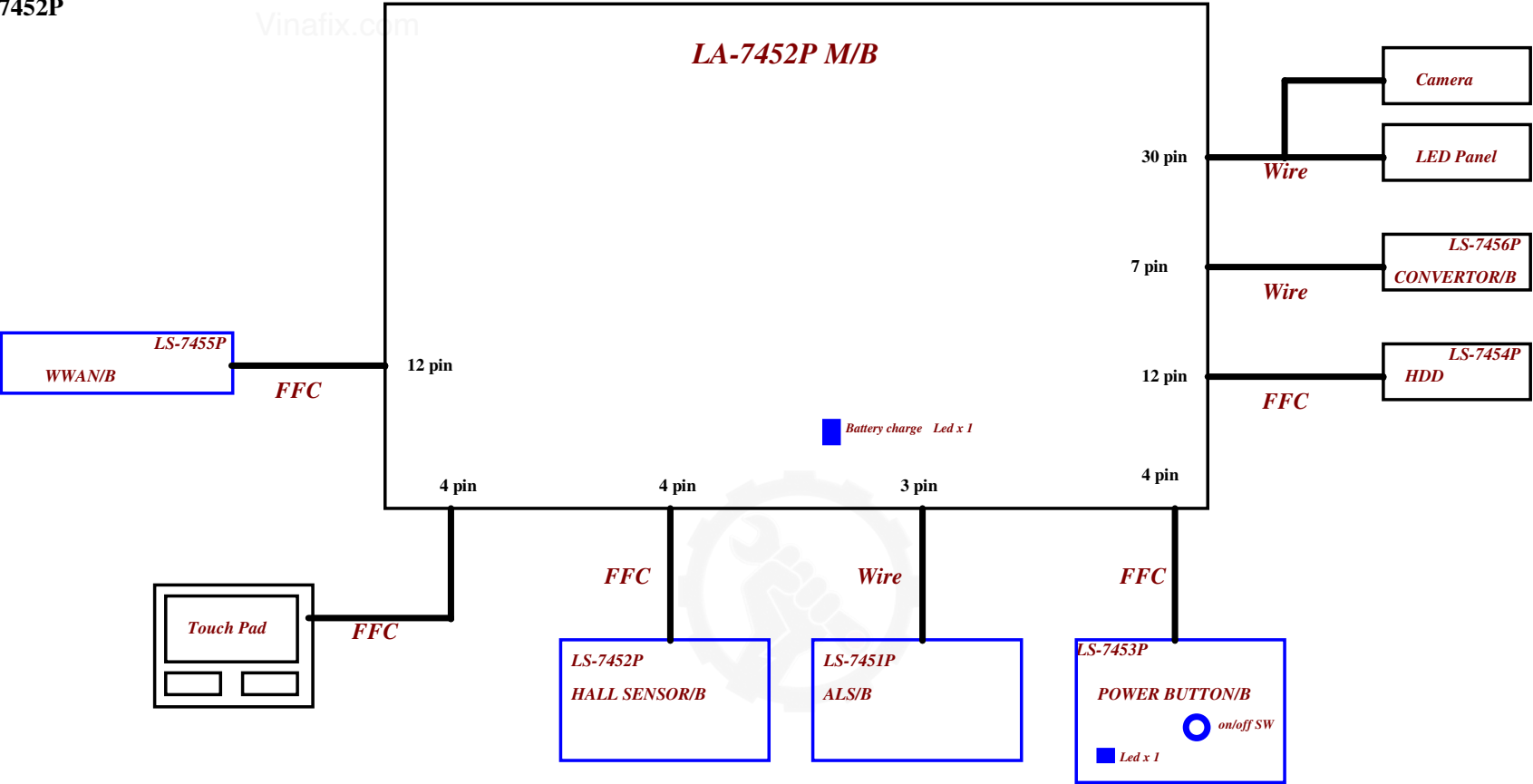
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Project Code : PLW00
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	SODIMM	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930												
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH											V	
MEM_SMBCLK MEM_SMBDATA	PCH				V	V		V					V

Link

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	A.0
4	
5	
6	
7	

PCH



USB PORT#	DESTINATION
0	None
1	JUSB1 (2.0 Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN/DMC)
6	ELC 8051
7	None
8	None
9	None
10	None
11	None
12	None
13	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

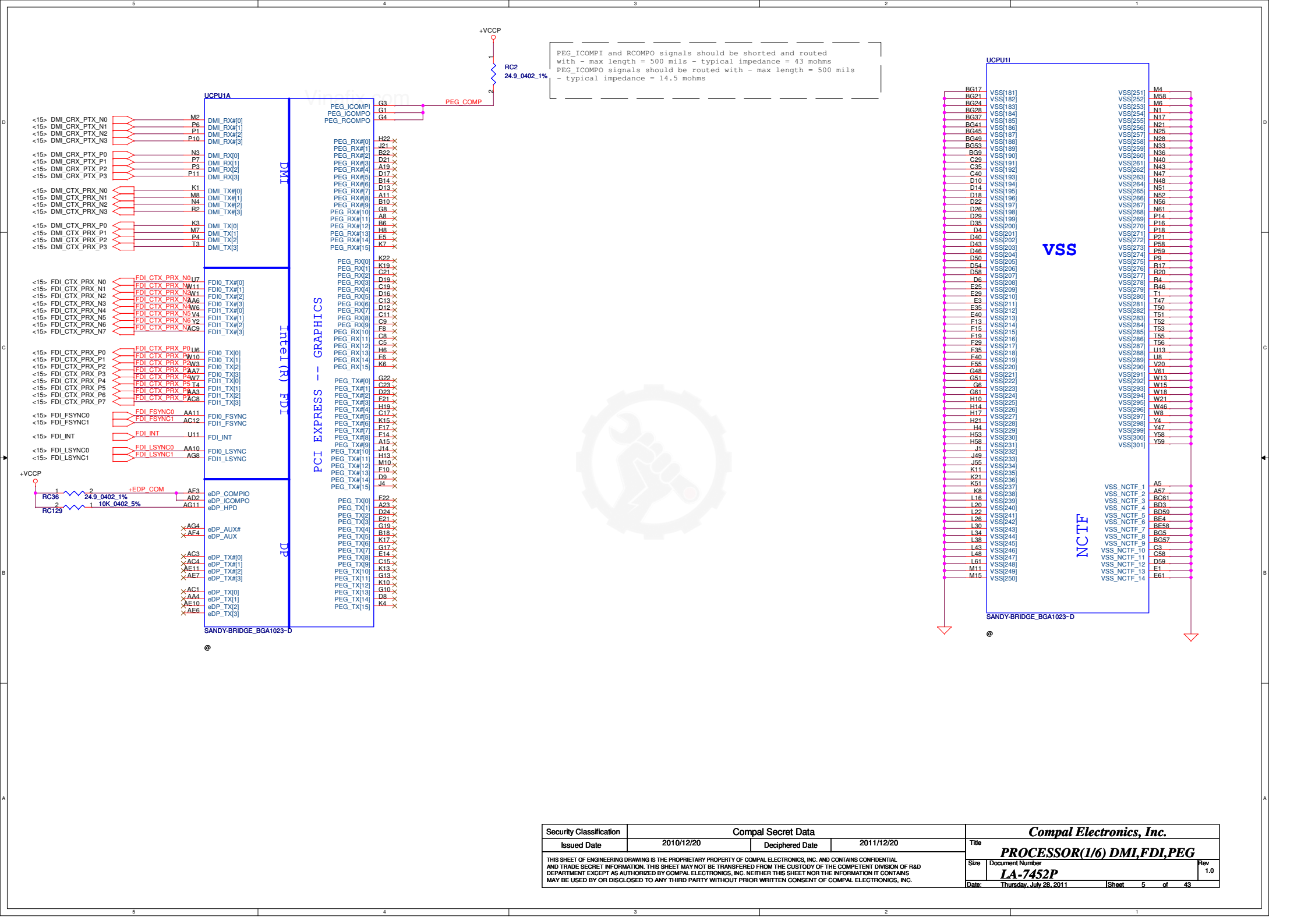
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

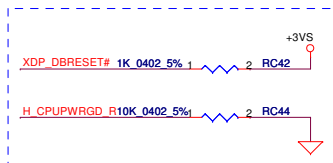
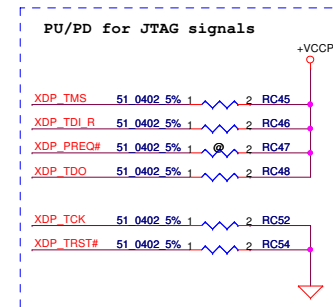
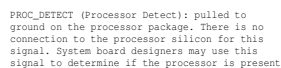
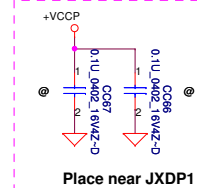
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

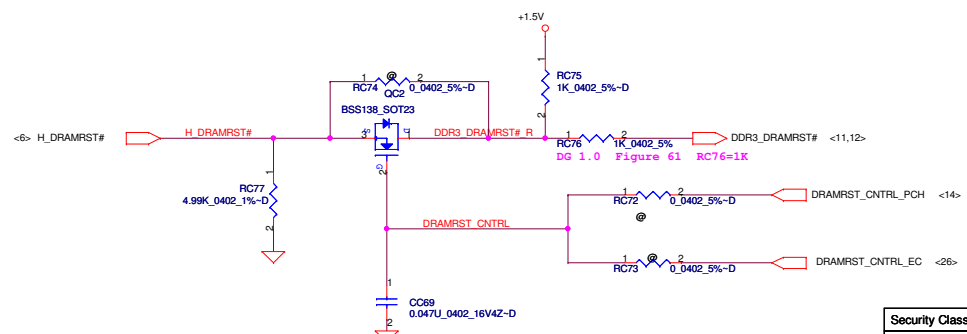
Symbol Note :

 : means Digital Ground
 : means Analog Ground

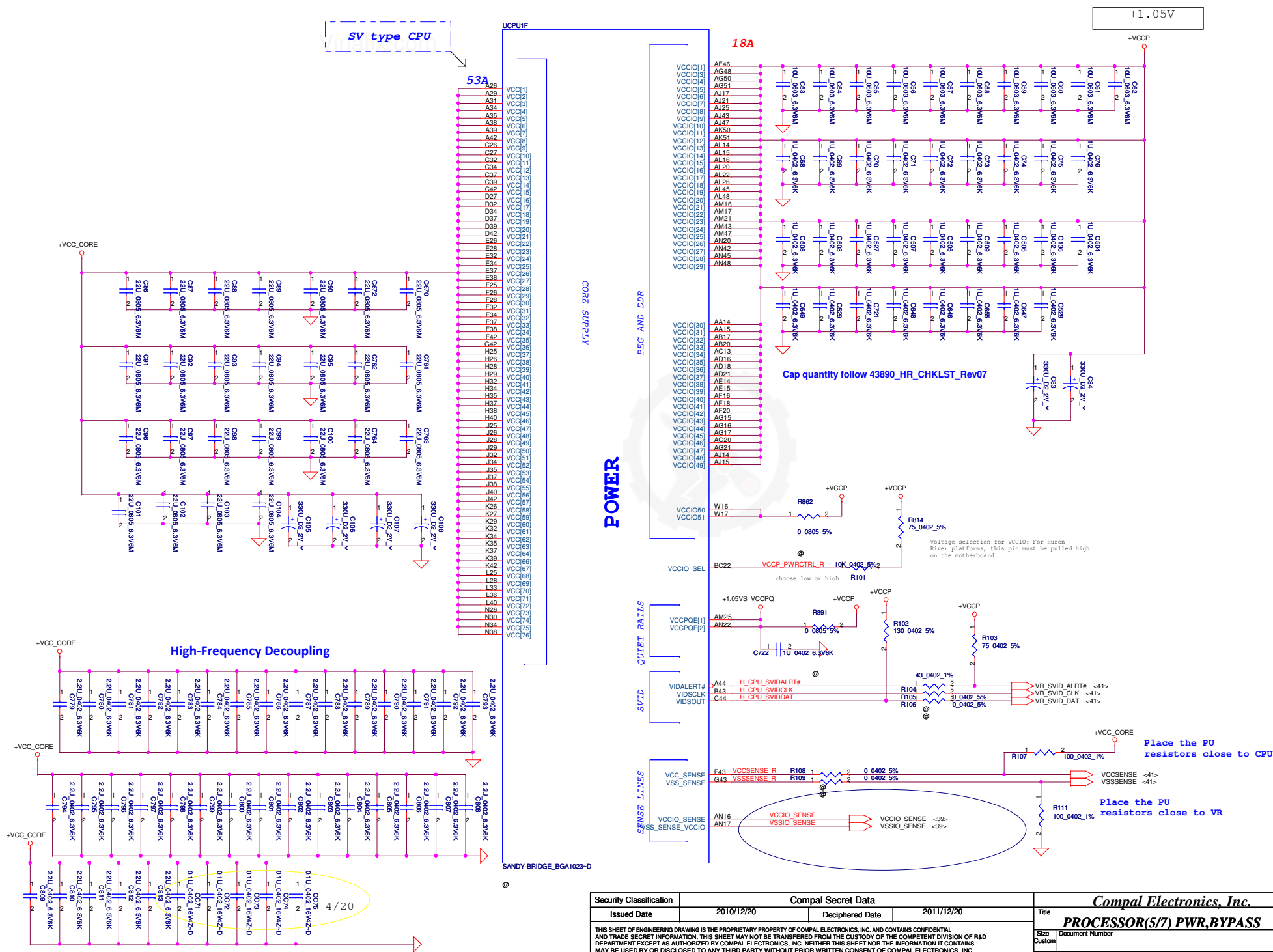
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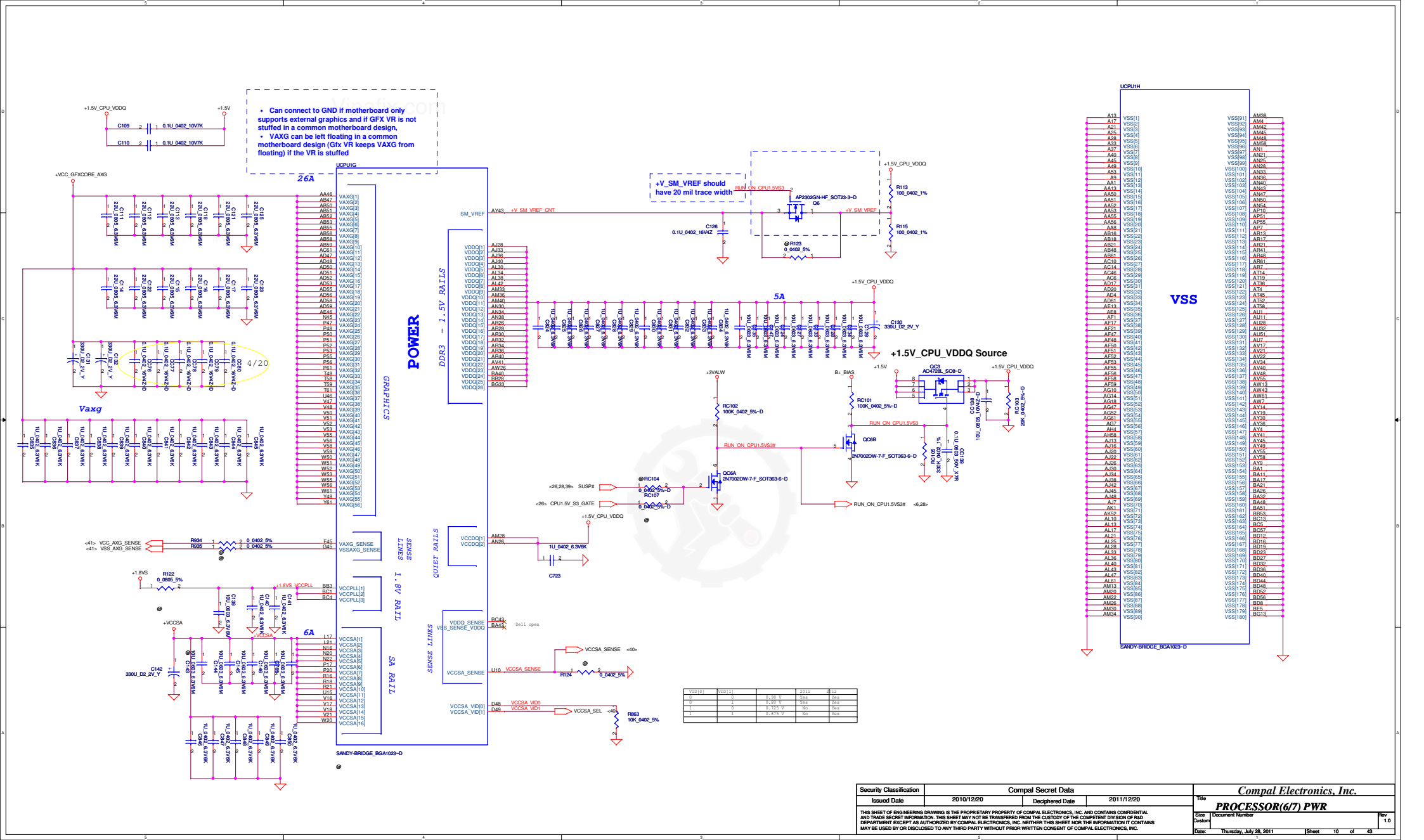


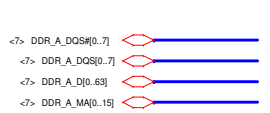


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Title			
PROCESSOR(3/6) DDRIII			
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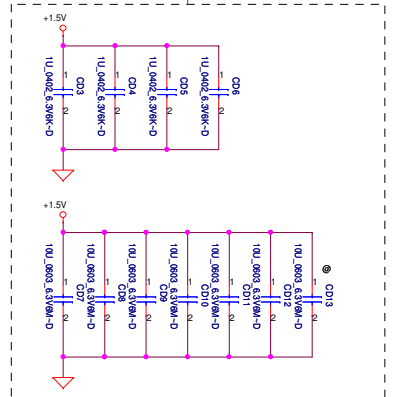
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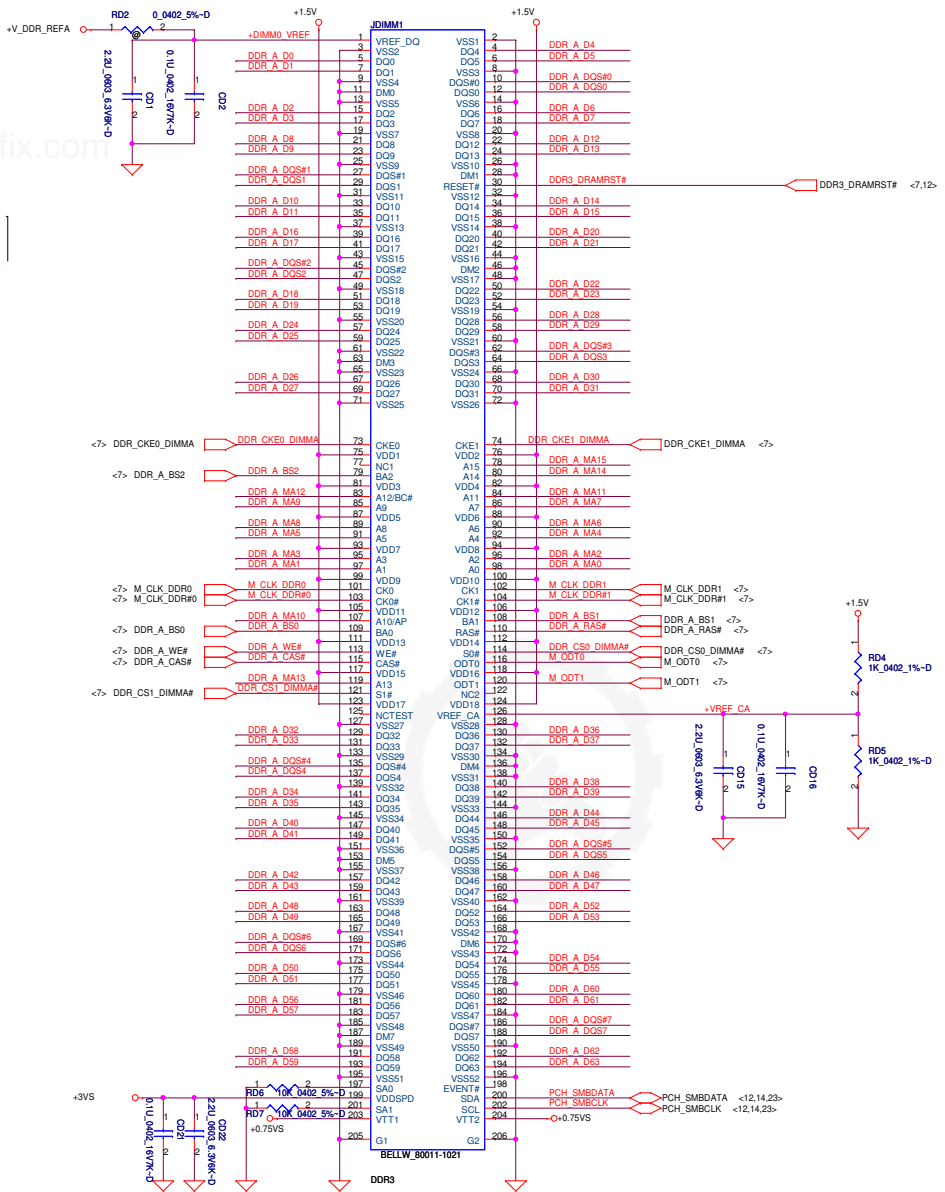
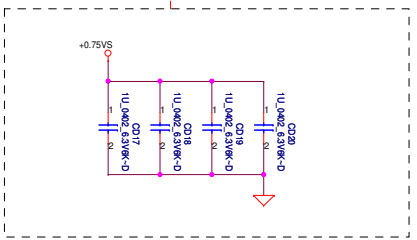


Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

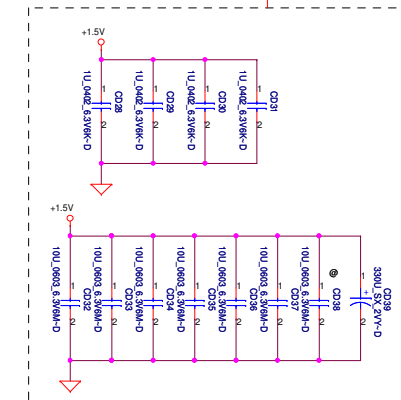


Layout Note:
Place near JDIMM1.203,204

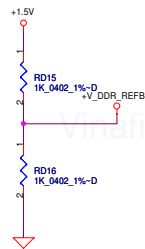
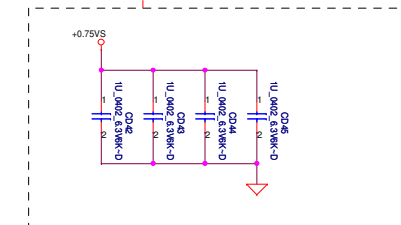


<7> DDR_B_DQS#[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_DQ[0..63]
<7> DDR_B_MA[0..15]

Layout Note:
Place near JDIMMB

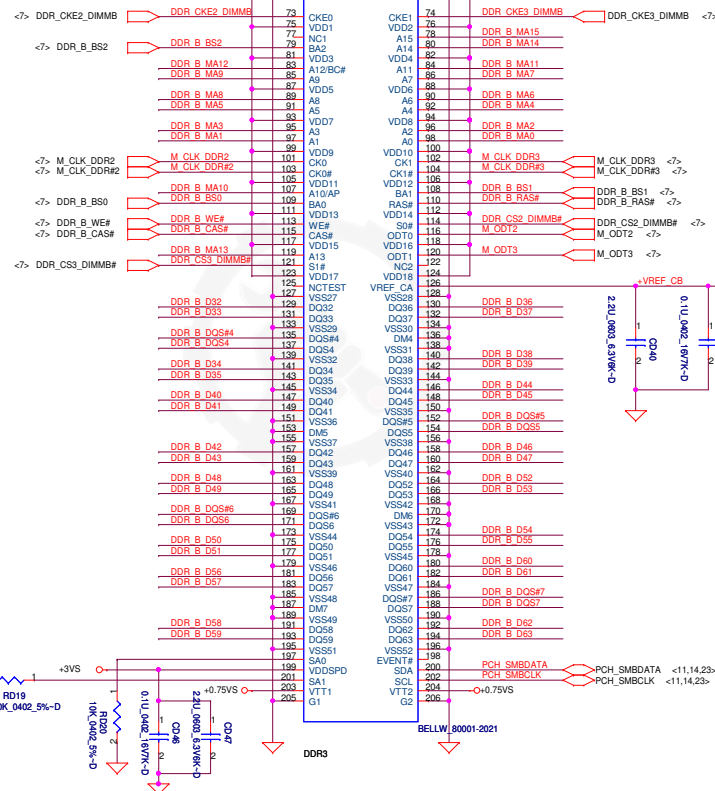


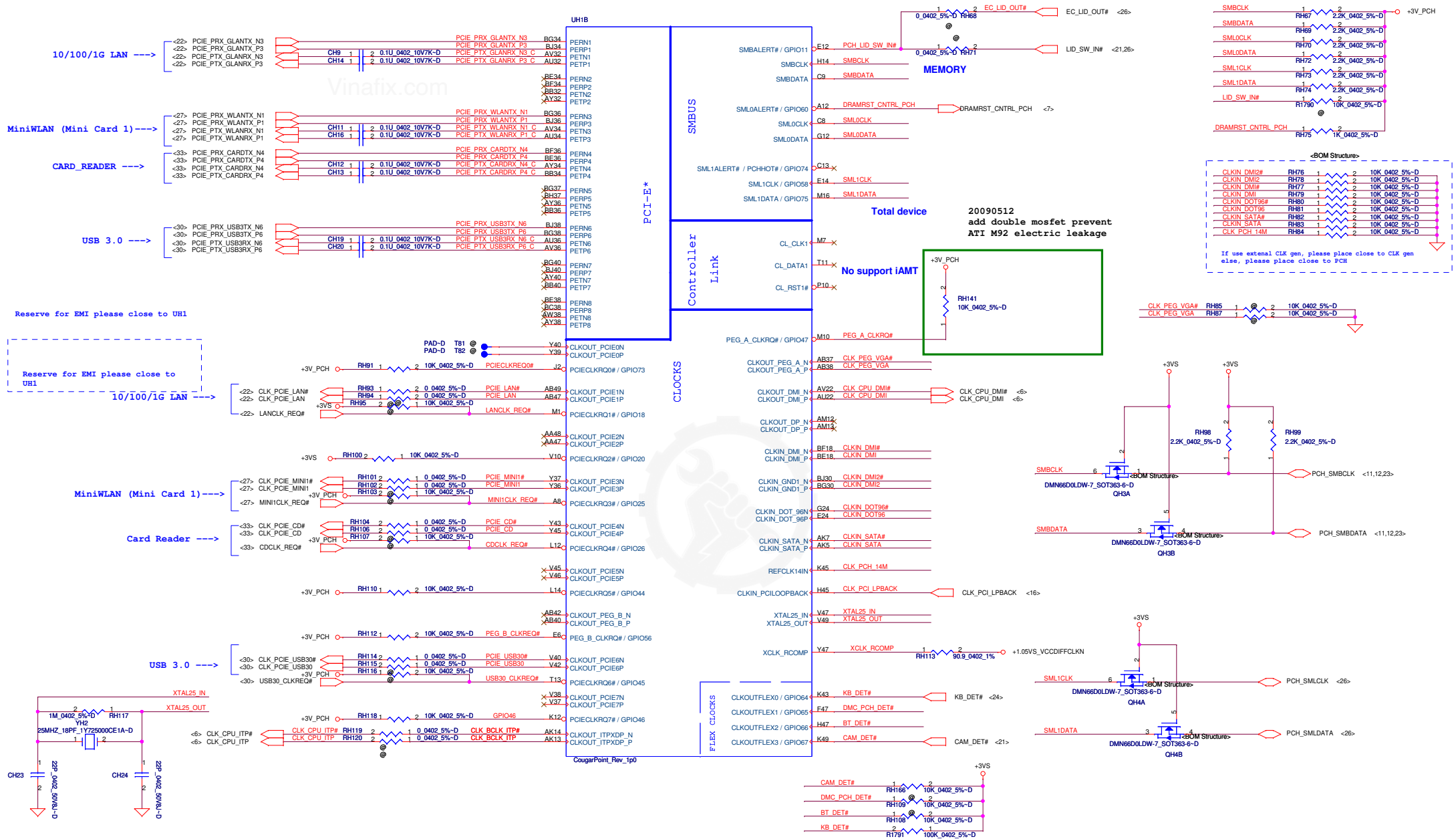
Layout Note:
Place near JDIMMB.203,204



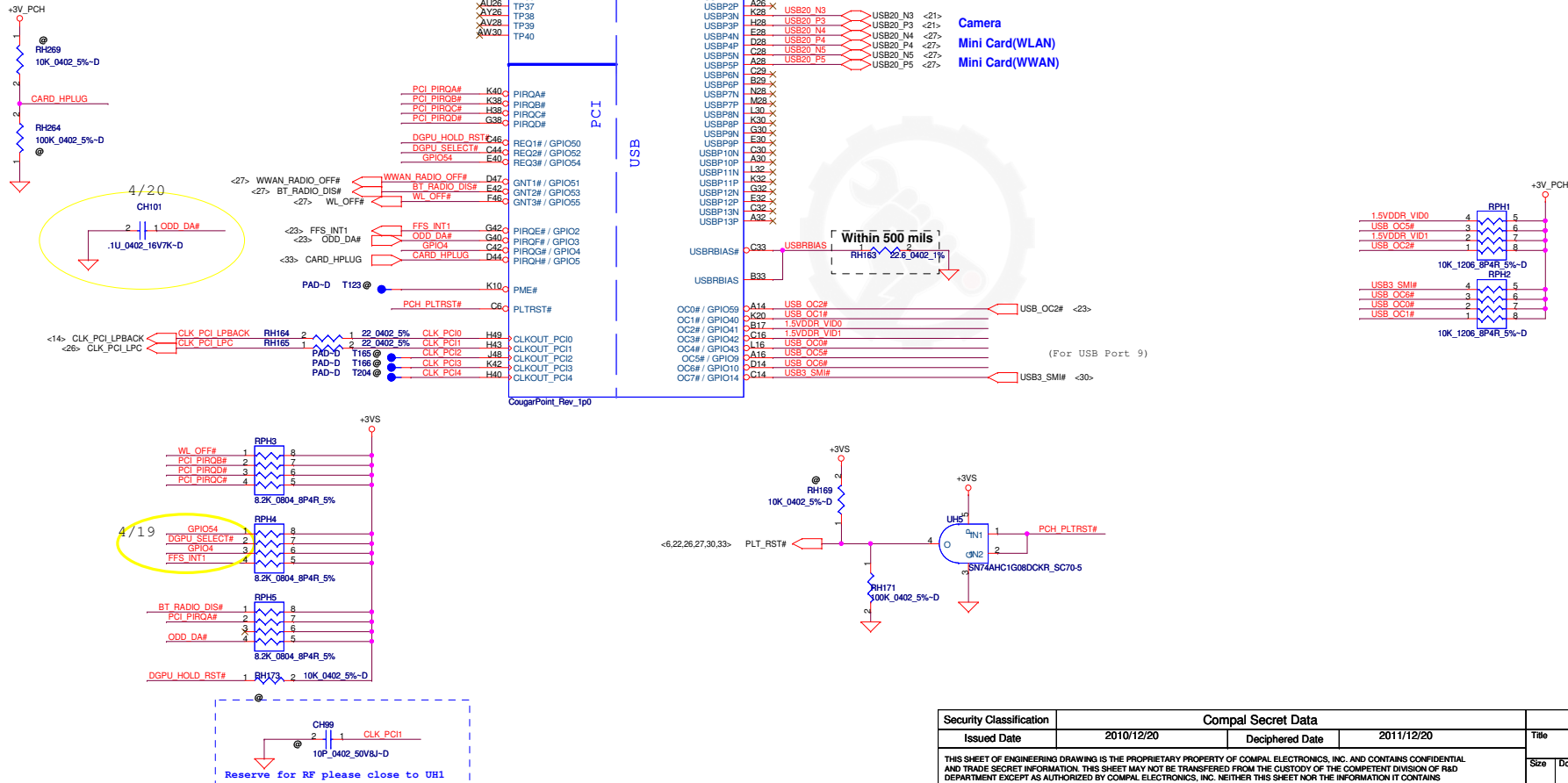
All VREF traces should
have 10 mil trace width

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



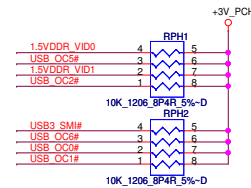


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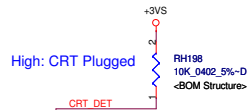
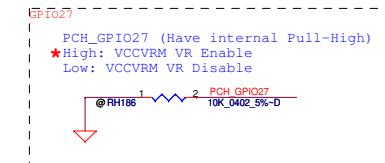
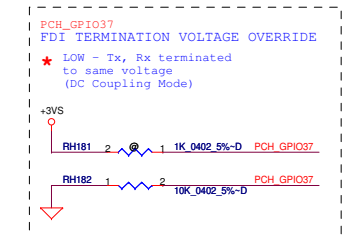
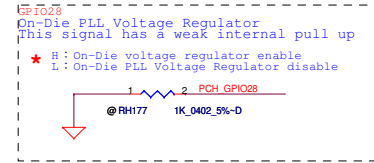


Intel Anti-Theft Technology	
NV_ALE	High=Endabled
	Low=Disable(floating) ★

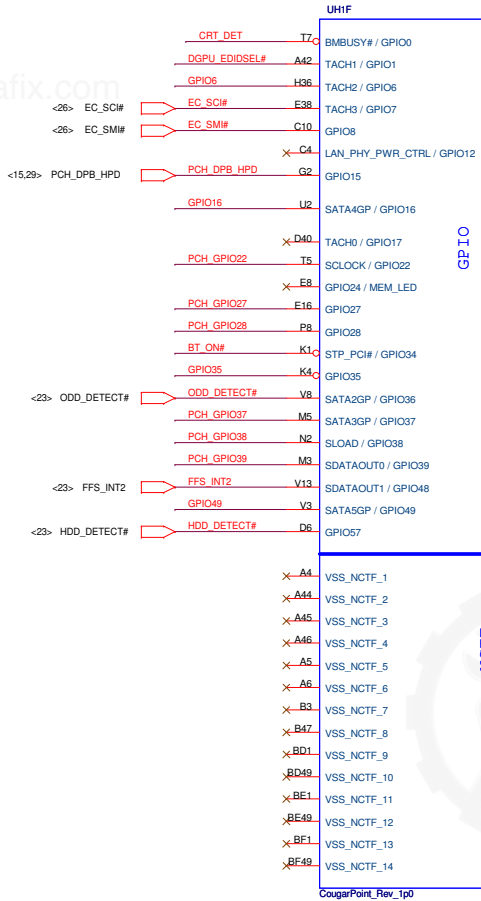
NV_ALE @ RH160 1 2 1K 0402 5%-D



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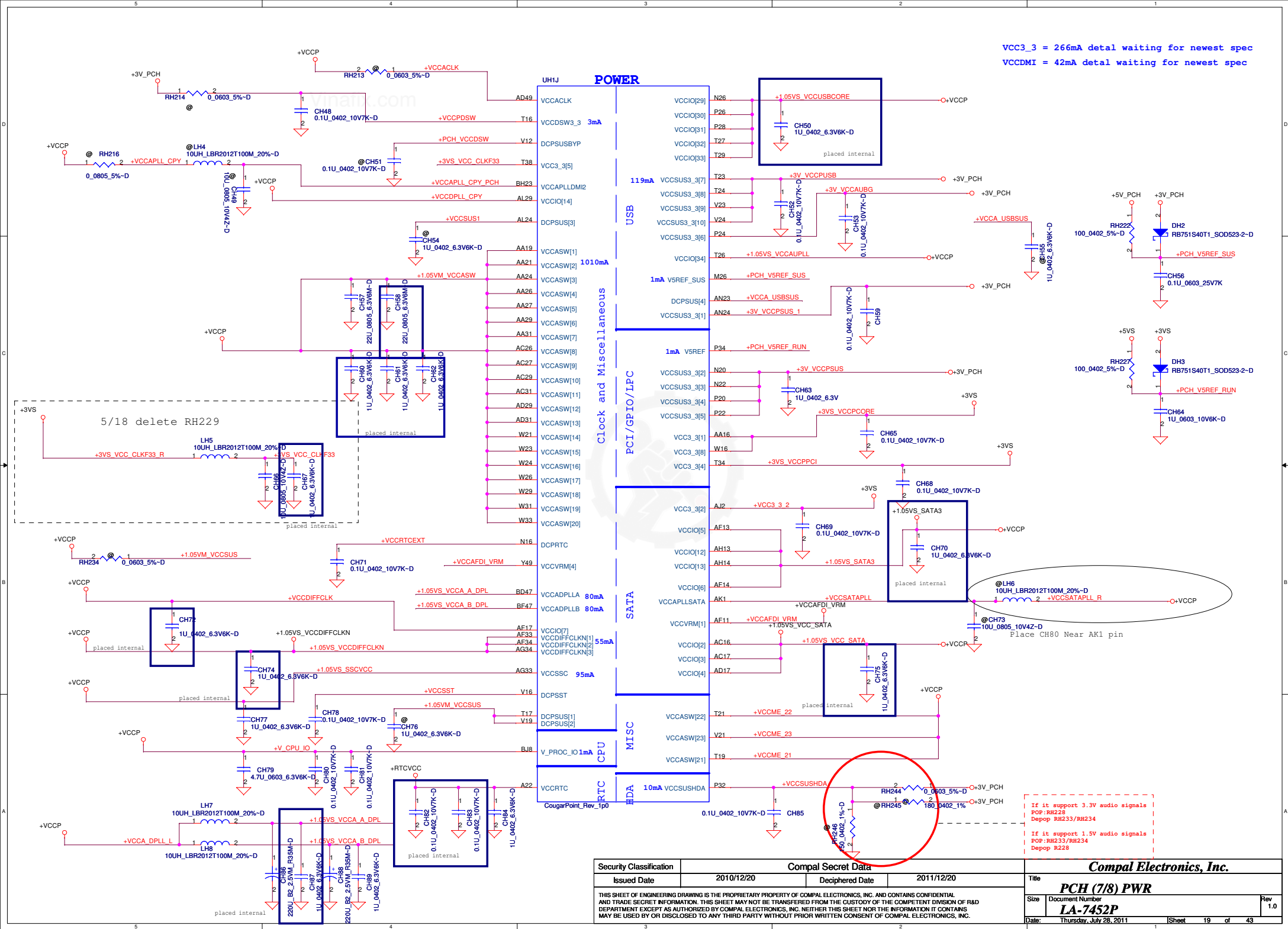
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

NC/F

CougarPoint_Rev_1p0

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UH1H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK6
AA34	VSS[5]	VSS[84] AL16
AB11	VSS[6]	VSS[85] AL17
AB14	VSS[7]	VSS[86] AL19
AB39	VSS[8]	VSS[87] AL2
AB4	VSS[9]	VSS[88] AL21
AB43	VSS[10]	VSS[89] AL23
AB5	VSS[11]	VSS[90] AL26
AB7	VSS[12]	VSS[91] AL27
AC19	VSS[13]	VSS[92] AL31
AC2	VSS[14]	VSS[93] AL33
AC21	VSS[15]	VSS[94] AL34
AC24	VSS[16]	VSS[95] AL46
AC33	VSS[17]	VSS[96] AM11
AC34	VSS[18]	VSS[97] AM14
AC48	VSS[19]	VSS[98] AM36
AD10	VSS[20]	VSS[99] AM39
AD11	VSS[21]	VSS[100] AM43
AD12	VSS[22]	VSS[101] AM45
AD13	VSS[23]	VSS[102] AM46
AD19	VSS[24]	VSS[103] AN2
AD24	VSS[25]	VSS[104] AN29
AD26	VSS[26]	VSS[105] AN3
AD27	VSS[27]	VSS[106] AP12
AD33	VSS[28]	VSS[107] AP19
AD34	VSS[29]	VSS[108] AP28
AD36	VSS[30]	VSS[109] AP30
AD37	VSS[31]	VSS[110] AP32
AD38	VSS[32]	VSS[111] AP4
AD39	VSS[33]	VSS[112] AP42
AD4	VSS[34]	VSS[113] AP46
AD40	VSS[35]	VSS[114] AP8
AD42	VSS[36]	VSS[115] AR2
AD43	VSS[37]	VSS[116] AR48
AD45	VSS[38]	VSS[117] AT11
AD46	VSS[39]	VSS[118] AT113
AD8	VSS[40]	VSS[119] AT18
AE2	VSS[41]	VSS[120] AT22
AE3	VSS[42]	VSS[121] AT28
AF10	VSS[43]	VSS[122] AT28
AF12	VSS[44]	VSS[123] AT30
AD14	VSS[45]	VSS[124] AT32
AF16	VSS[46]	VSS[125] AT34
AF19	VSS[47]	VSS[126] AT39
AF24	VSS[48]	VSS[127] AT42
AF26	VSS[49]	VSS[128] AT46
AF27	VSS[50]	VSS[129] AT7
AF29	VSS[51]	VSS[130] AU20
AF31	VSS[52]	VSS[131] AU30
AF38	VSS[53]	VSS[132] AV16
AF4	VSS[54]	VSS[133] AV20
VSS[55]	VSS[55]	VSS[134] AV24
AF42	VSS[56]	VSS[135] AV30
AF46	VSS[57]	VSS[136] AV38
AF5	VSS[58]	VSS[137] AV4
AF7	VSS[59]	VSS[138] AV43
AF8	VSS[60]	VSS[139] AV8
AG19	VSS[61]	VSS[140] AW14
AG2	VSS[62]	VSS[141] AW18
AG31	VSS[63]	VSS[142] AW2
AG48	VSS[64]	VSS[143] AW22
AH11	VSS[65]	VSS[144] AW26
AH3	VSS[66]	VSS[145] AW28
AH36	VSS[67]	VSS[146] AW32
AH38	VSS[68]	VSS[147] AW36
AH40	VSS[69]	VSS[148] AW40
AH42	VSS[70]	VSS[149] AW48
AH46	VSS[71]	VSS[150] AW4
AH7	VSS[72]	VSS[151] AW24
AJ19	VSS[73]	VSS[152] AW36
AJ21	VSS[74]	VSS[153] AW40
AJ24	VSS[75]	VSS[154] AW48
AJ33	VSS[76]	VSS[155] AY12
AJ34	VSS[77]	VSS[156] AY22
AK12	VSS[78]	VSS[157] AY28
AK3	VSS[79]	VSS[158]

CougarPoint_Rev_1p0

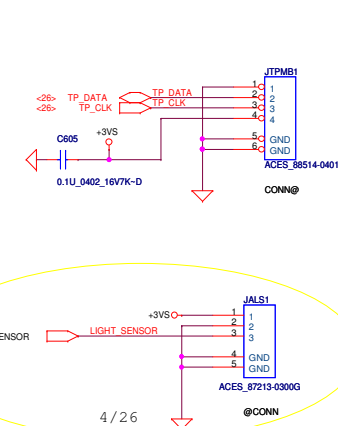
UH1I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B39	VSS[169]	VSS[269] L38
B7	VSS[170]	VSS[270] L48
F45	VSS[171]	VSS[271] M12
BB12	VSS[172]	VSS[272] M18
BB16	VSS[173]	VSS[273] M22
BB20	VSS[174]	VSS[274] M24
BB22	VSS[175]	VSS[275] M30
BB24	VSS[176]	VSS[276] M32
BB28	VSS[177]	VSS[277] M34
BB30	VSS[178]	VSS[278] M38
BB38	VSS[179]	VSS[279] M4
BB4	VSS[180]	VSS[280] M42
BB46	VSS[181]	VSS[281] M46
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] M8
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] N47
BC26	VSS[187]	VSS[287] P11
BC32	VSS[188]	VSS[288] P18
BC34	VSS[189]	VSS[289] T33
AM7	VSS[190]	VSS[290] P40
BC40	VSS[191]	VSS[291] P43
BC42	VSS[192]	VSS[292] P47
BC48	VSS[193]	VSS[293] R2
BD46	VSS[194]	VSS[294] R48
BD5	VSS[195]	VSS[295] T12
BE22	VSS[196]	VSS[296] T31
BE26	VSS[197]	VSS[297] T4
BE40	VSS[198]	VSS[298] T4
BF12	VSS[199]	VSS[299] W34
BF16	VSS[200]	VSS[300] T46
BF20	VSS[201]	VSS[301] T8
BF22	VSS[202]	VSS[302] V11
BF24	VSS[203]	VSS[303] V17
BF26	VSS[204]	VSS[304] V26
BF28	VSS[205]	VSS[305] V38
BF30	VSS[206]	VSS[306] V43
BF30	VSS[207]	VSS[307] V7
BF38	VSS[208]	VSS[308] W17
BF40	VSS[209]	VSS[309] W19
BF48	VSS[210]	VSS[310] W2
BF8	VSS[211]	VSS[311] W27
BG17	VSS[212]	VSS[312] W48
BG21	VSS[213]	VSS[313] Y12
BG33	VSS[214]	VSS[314] Y4
BG44	VSS[215]	VSS[315] Y46
BG8	VSS[216]	VSS[316] Y8
BH11	VSS[217]	VSS[317] Y8
BH15	VSS[218]	VSS[318] Y8
BH17	VSS[219]	VSS[319] Y8
BH19	VSS[220]	VSS[320] Y8
H10	VSS[221]	VSS[321] Y8
BH27	VSS[222]	VSS[322] Y8
BH31	VSS[223]	VSS[323] Y8
BH33	VSS[224]	VSS[324] Y8
BH35	VSS[225]	VSS[325] Y8
BH39	VSS[226]	VSS[326] Y8
BH43	VSS[227]	VSS[327] Y8
BH7	VSS[228]	VSS[328] Y8
D1	VSS[229]	VSS[329] Y8
D12	VSS[230]	VSS[330] Y8
D16	VSS[231]	VSS[331] Y8
D18	VSS[232]	VSS[332] Y8
D22	VSS[233]	VSS[333] Y8
D24	VSS[234]	VSS[334] Y8
D26	VSS[235]	VSS[335] Y8
D30	VSS[236]	VSS[336] Y8
D32	VSS[237]	VSS[337] Y8
D34	VSS[238]	VSS[338] Y8
D38	VSS[239]	VSS[339] Y8
D42	VSS[240]	VSS[340] Y8
D8	VSS[241]	VSS[341] Y8
E18	VSS[242]	VSS[342] Y8
E26	VSS[243]	VSS[343] Y8
G18	VSS[244]	VSS[344] Y8
G20	VSS[245]	VSS[345] Y8
G26	VSS[246]	VSS[346] Y8
G28	VSS[247]	VSS[347] Y8
G36	VSS[248]	VSS[348] Y8
H12	VSS[249]	VSS[349] Y8
H18	VSS[250]	VSS[350] Y8
H22	VSS[251]	VSS[351] Y8
H24	VSS[252]	VSS[352] Y8
H26	VSS[253]	VSS[353] Y8
H30	VSS[254]	VSS[354] Y8
H32	VSS[255]	VSS[355] Y8
H34	VSS[256]	VSS[356] Y8
F3	VSS[257]	VSS[357] Y8
VSS[258]	VSS[258]	VSS[358] Y8

CougarPoint_Rev_1p0

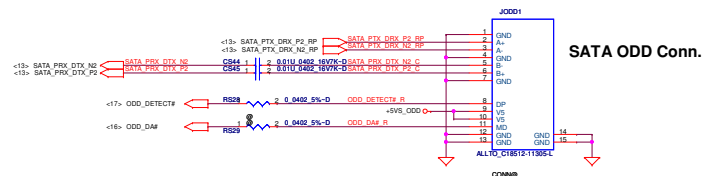
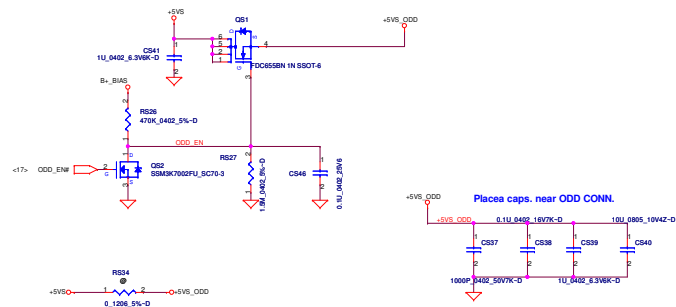
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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	PCH (8/8) VSS
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PWR BTN Board CONN

close to JTPMB 7/26


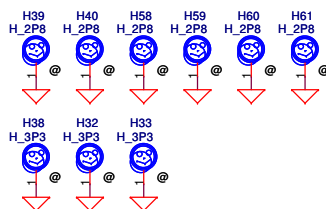
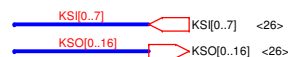


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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	VGA / LVDS /camera conn.	
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[illegible][illegible]

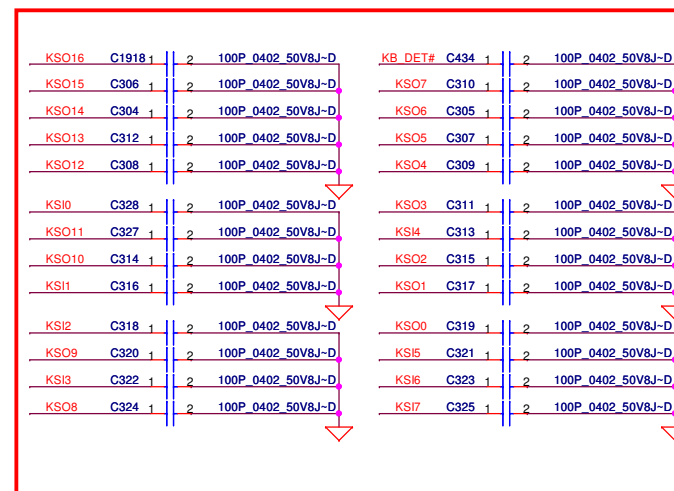
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Issued Date	2010/11/20	Deciphered Date	2011/11/20	
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Power Button

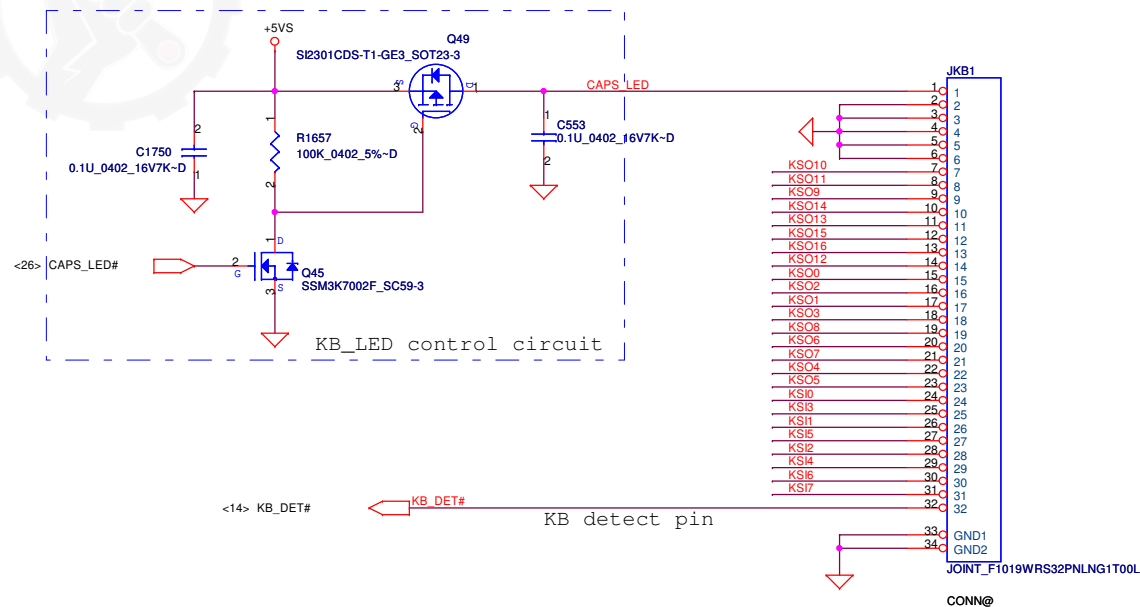


zzz

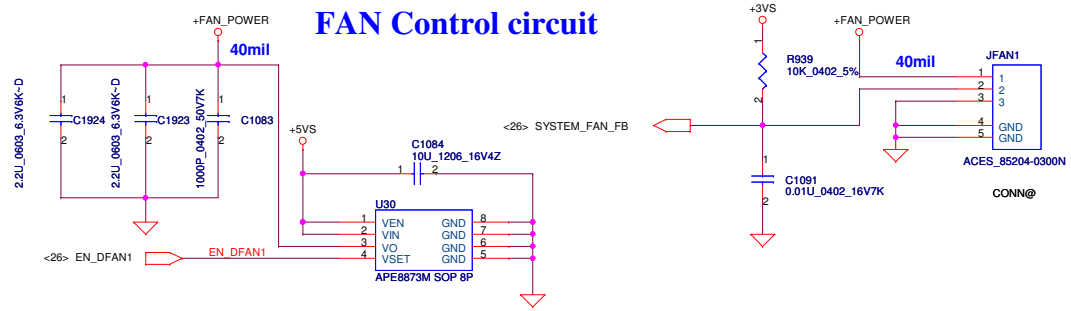
PCB-MB



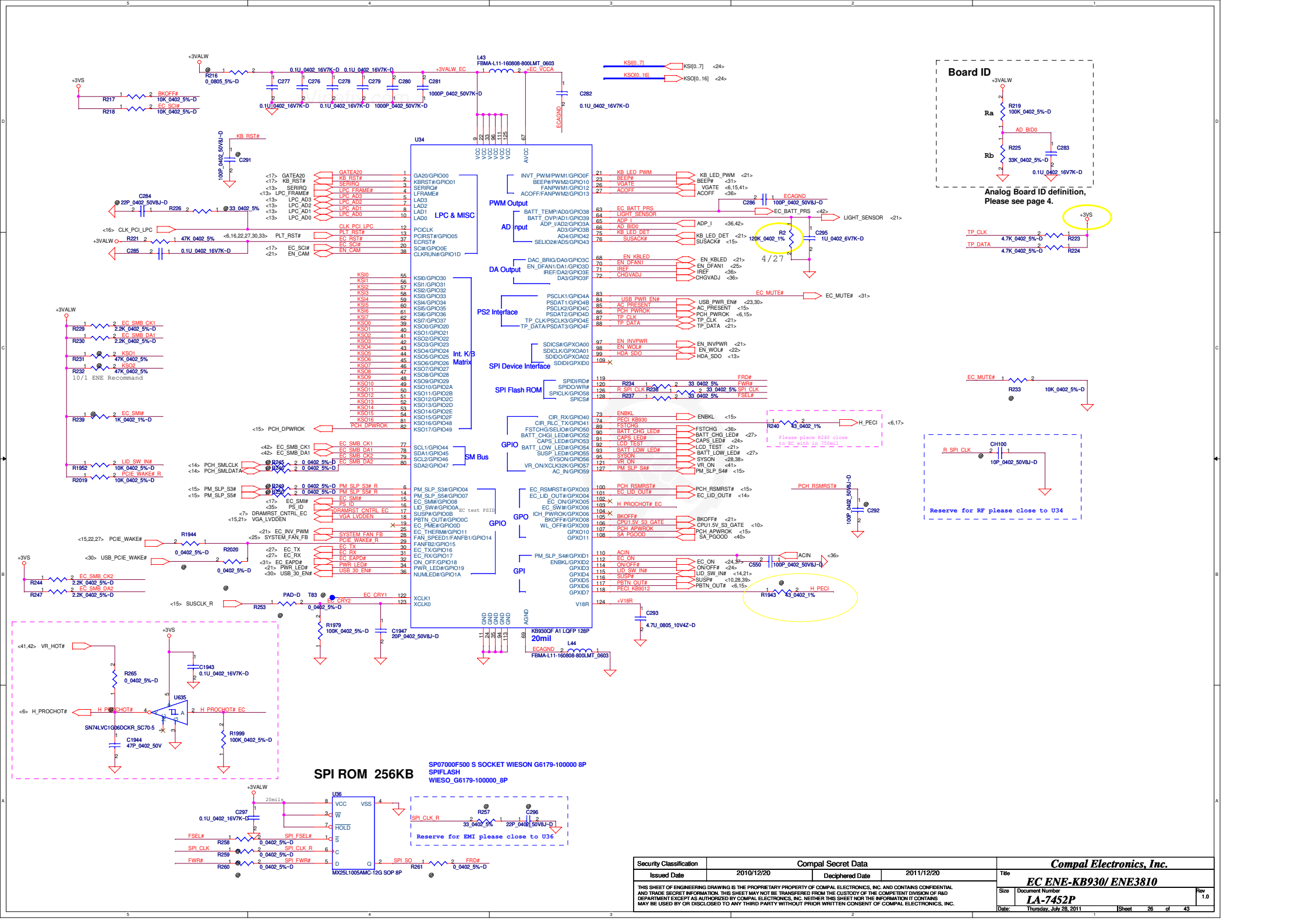
INT_KBD Conn.

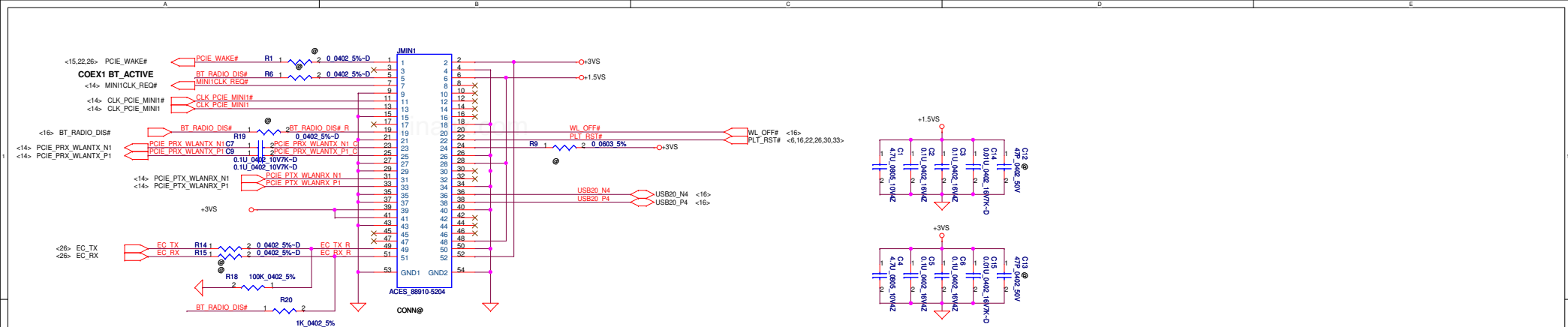


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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	
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				Size	Rev
				Document Number LA-7452P	1.0
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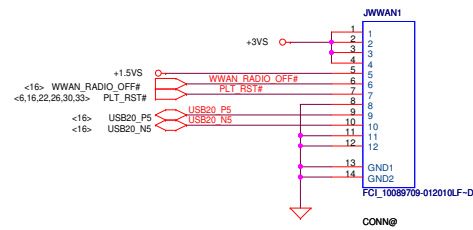
FAN Control circuit

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	
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				Size	Document Number
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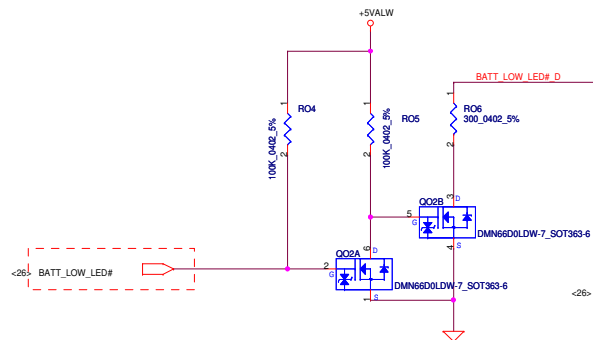




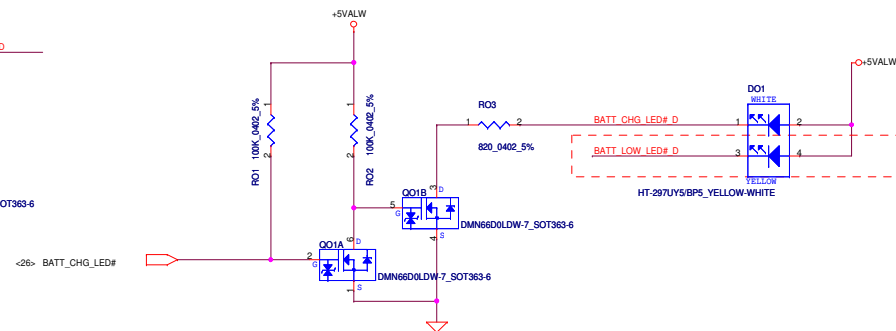
TO WLAN BOARD



BATT LOW

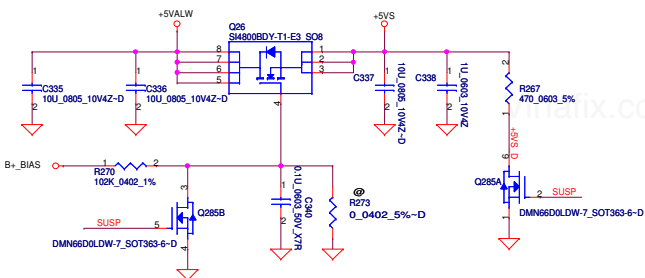


BATT CHARGE

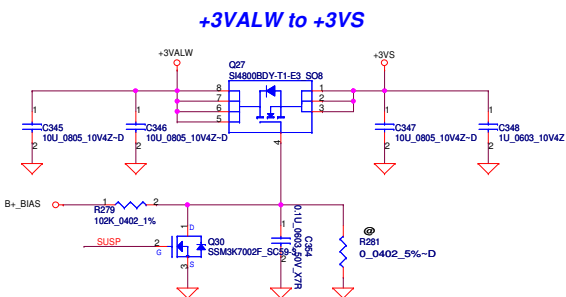


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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title	
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				Size	Document Number
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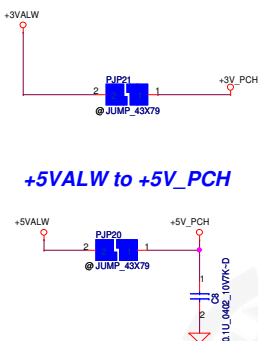
+5VALW to +5VS



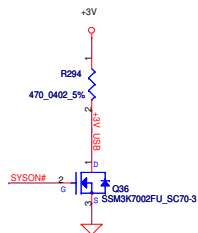
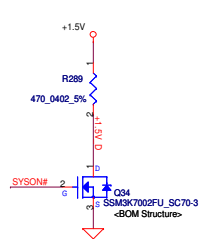
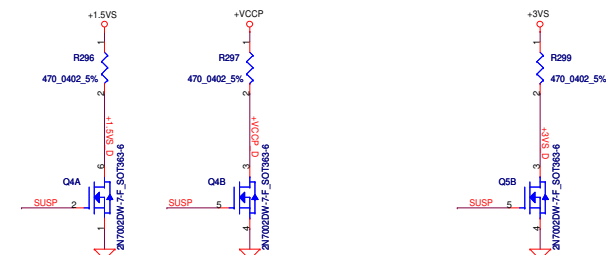
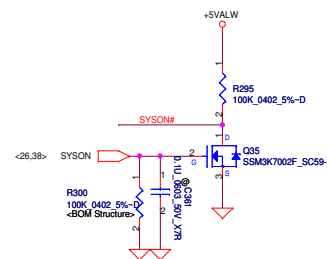
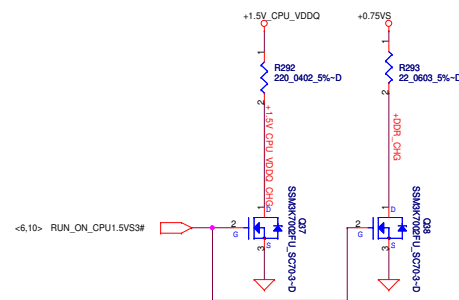
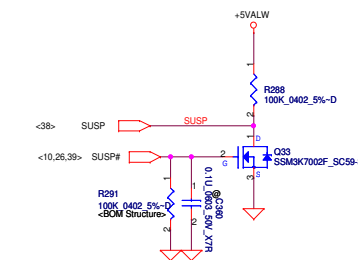
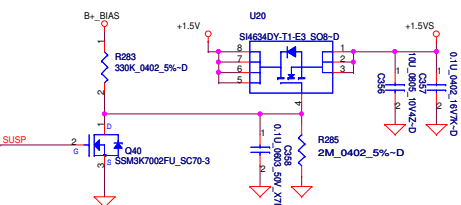
+3VALW to +3V_PCH



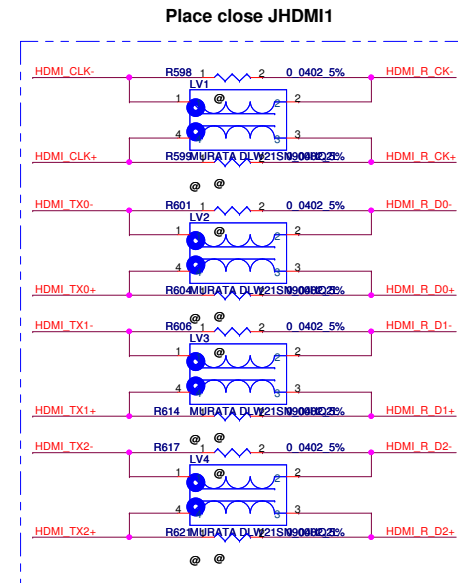
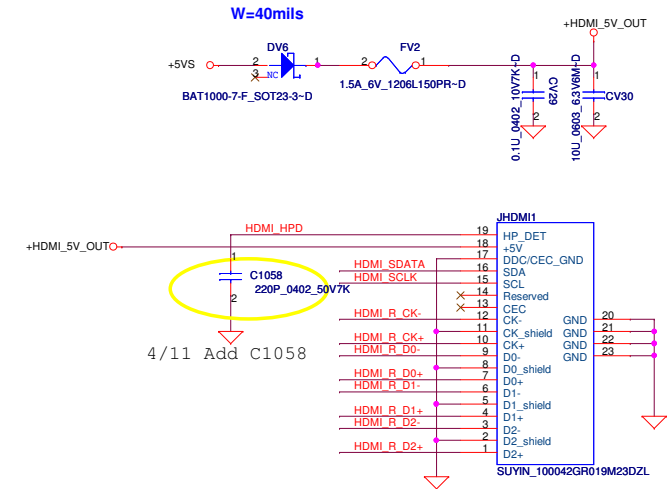
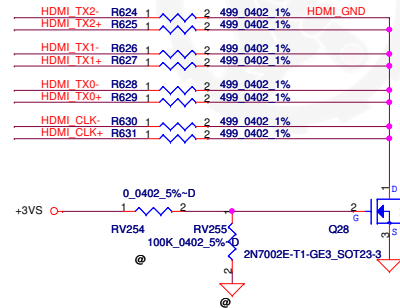
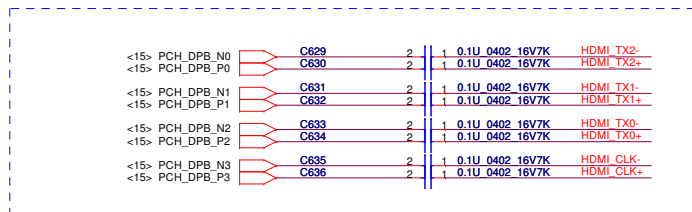
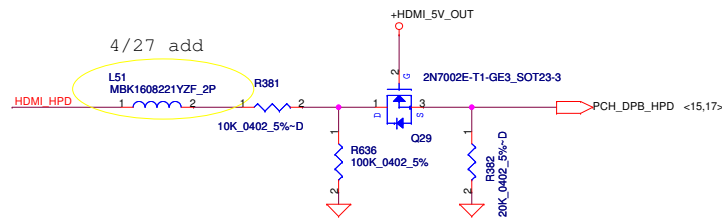
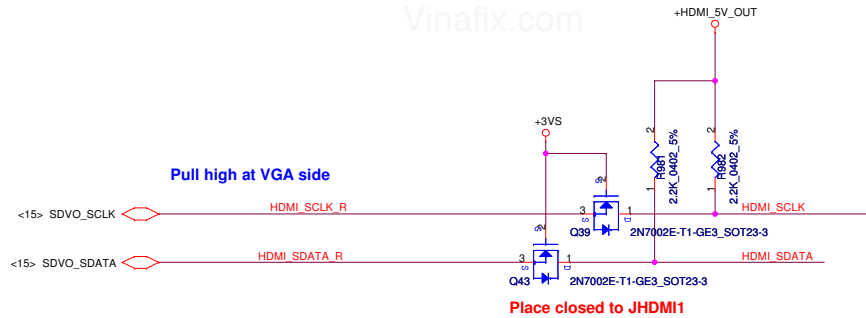
+5VALW to +5V_PCH



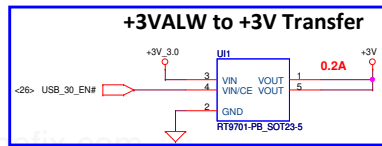
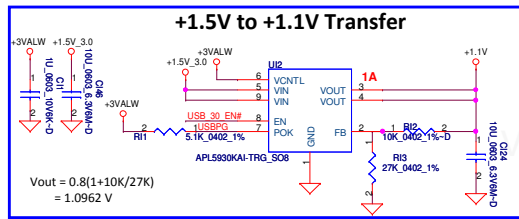
+1.5V To +1.5VS



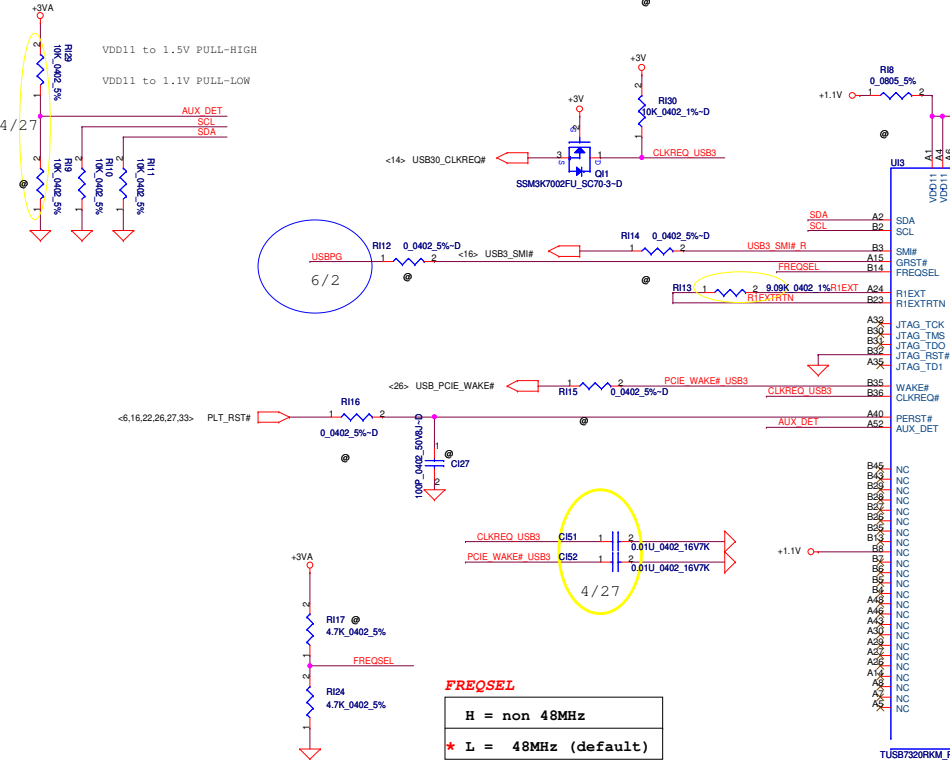
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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title DC/DC Interface	
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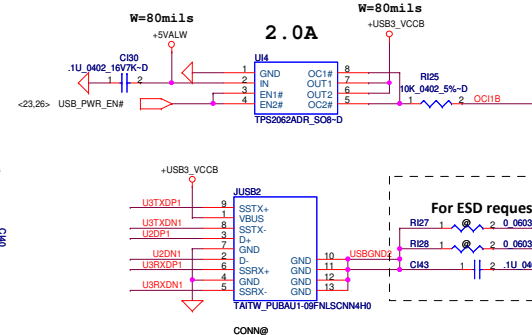
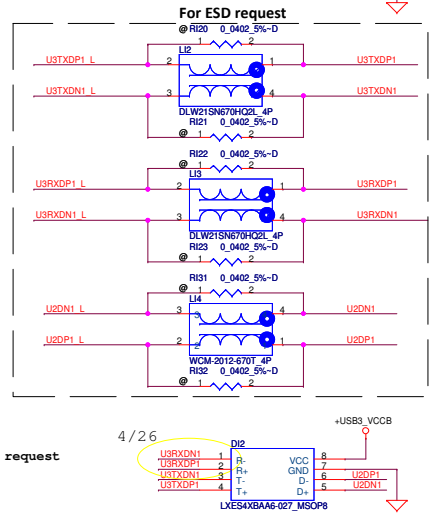
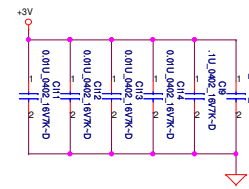
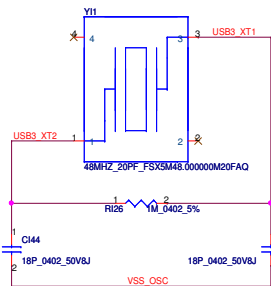
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				Size	Document Number
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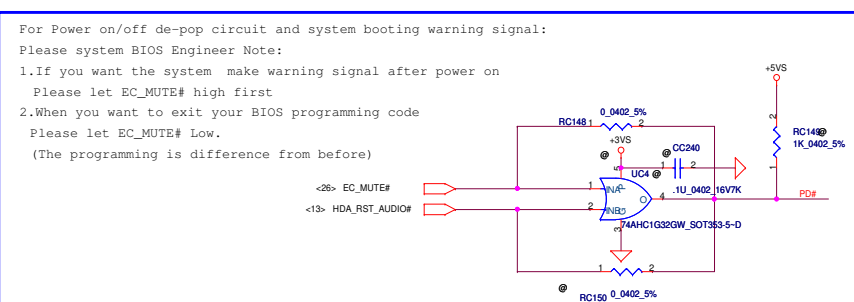
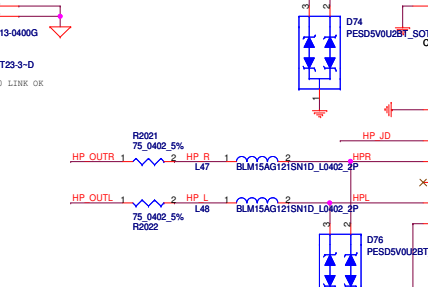
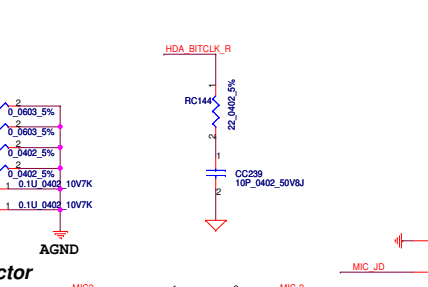
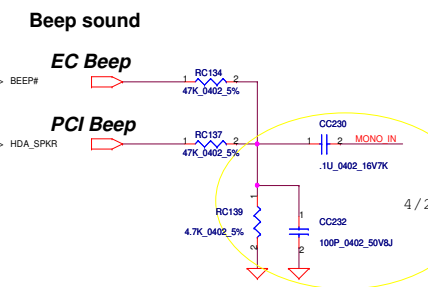
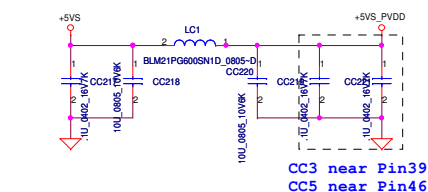
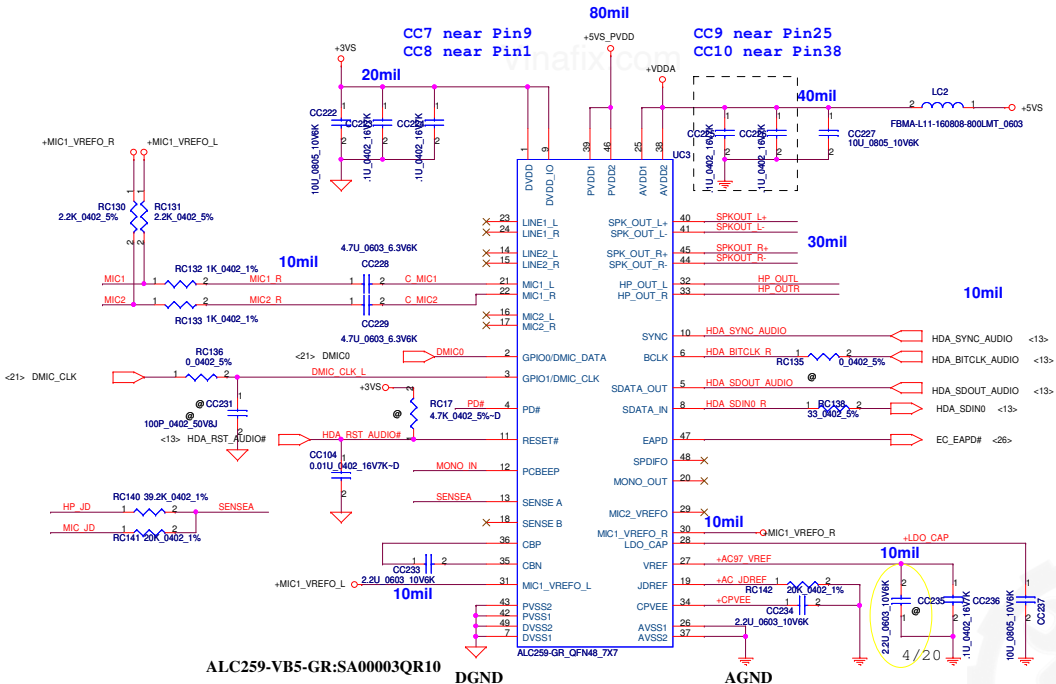


7K for customer request, can use other kind of capacitor, like Y5V.



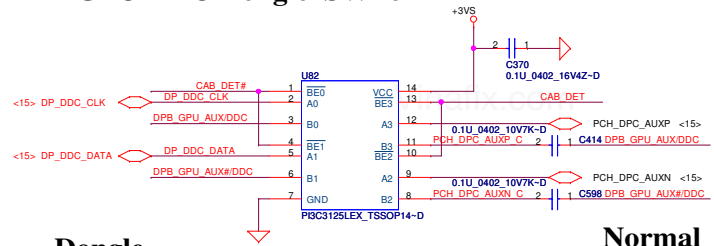
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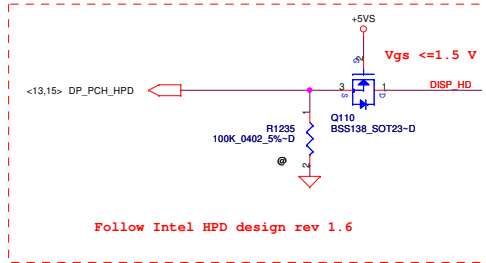
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GPU DDC Dongle SW for DP



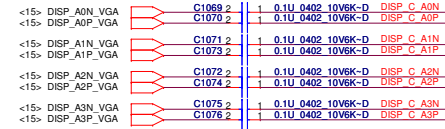
Dongle

Normal

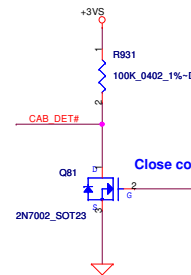
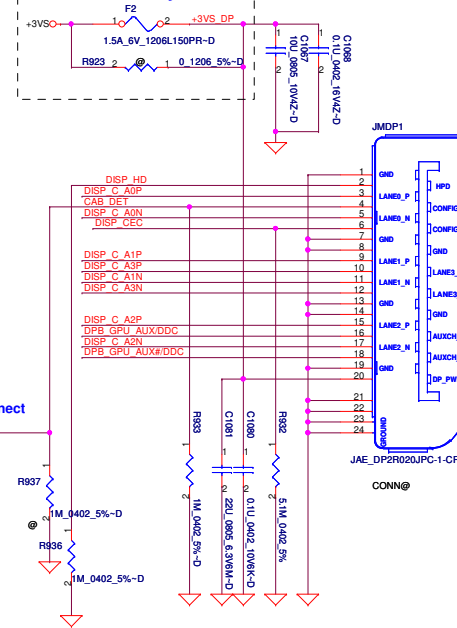


Follow Intel HPD design rev 1.6

Near to PCH



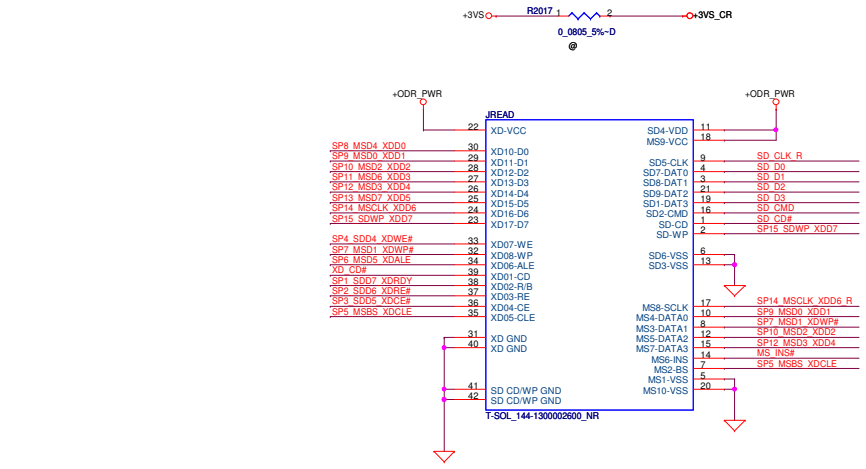
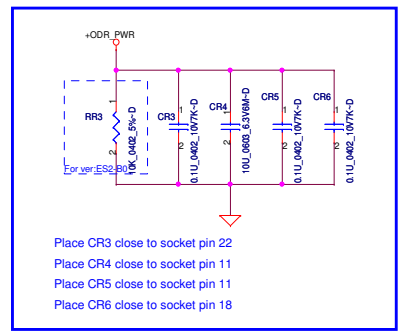
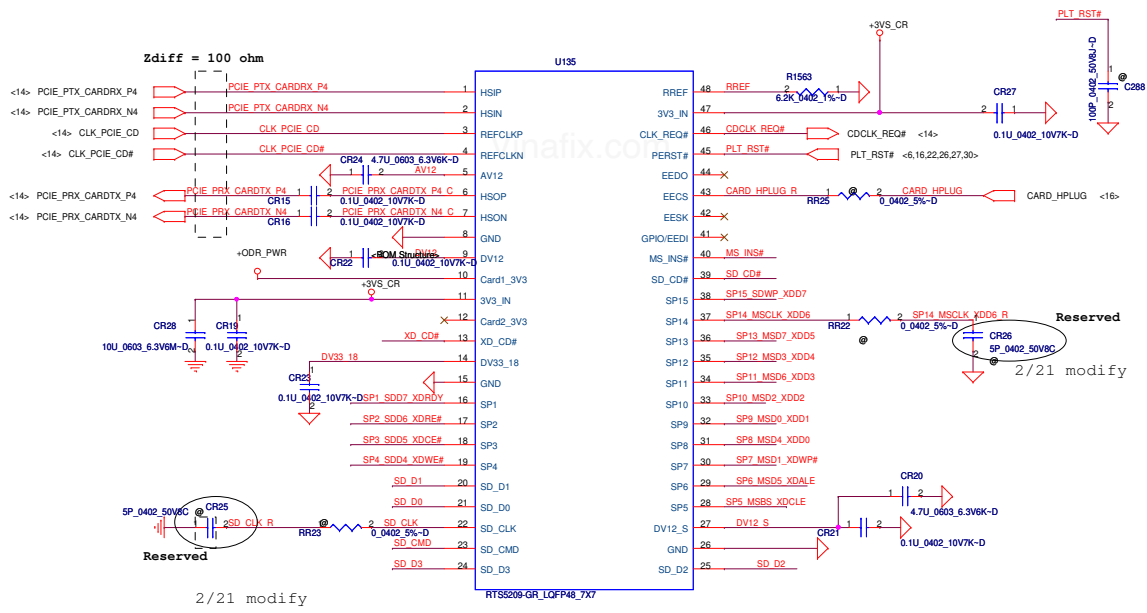
Co-lay



Close connect

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Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	KB930A TO KB9012					
2						
3						
4						
5						
6						
7						
8						
9						
10						

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Issued Date		Deciphered Date		Title	
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$$\text{ADP I} = 19.9 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$

ADP_1 19.9 uAadapcel-Rsense

CP mode

$I_{input} = (1/0.02) (0.05 \cdot V_{ac1m} / 2.39 + 0.05)$

$V_{ac1m} = 2.39 \cdot ((20.5K / 152K) / ((10K / 152K) + (20.5K / 152K)))$

CC=2.8A

$I_{REF} = 1 \cdot I_{charge}$

$I_{REF} = 0.25V \sim 2.8V$

CHGVADJ CV mode

$$\begin{aligned} I_{\text{input}} &= (1/0.02) (0.05 \cdot V_{\text{aclm}}/2.39 + 0.05) \\ V_{\text{aclm}} &= 2.39 \cdot ((20.5\text{K}/152\text{K}) / ((10\text{K}/152\text{K}) + (20.5\text{K}/152\text{K}))) \end{aligned}$$

IREF=0.25V~2.8V

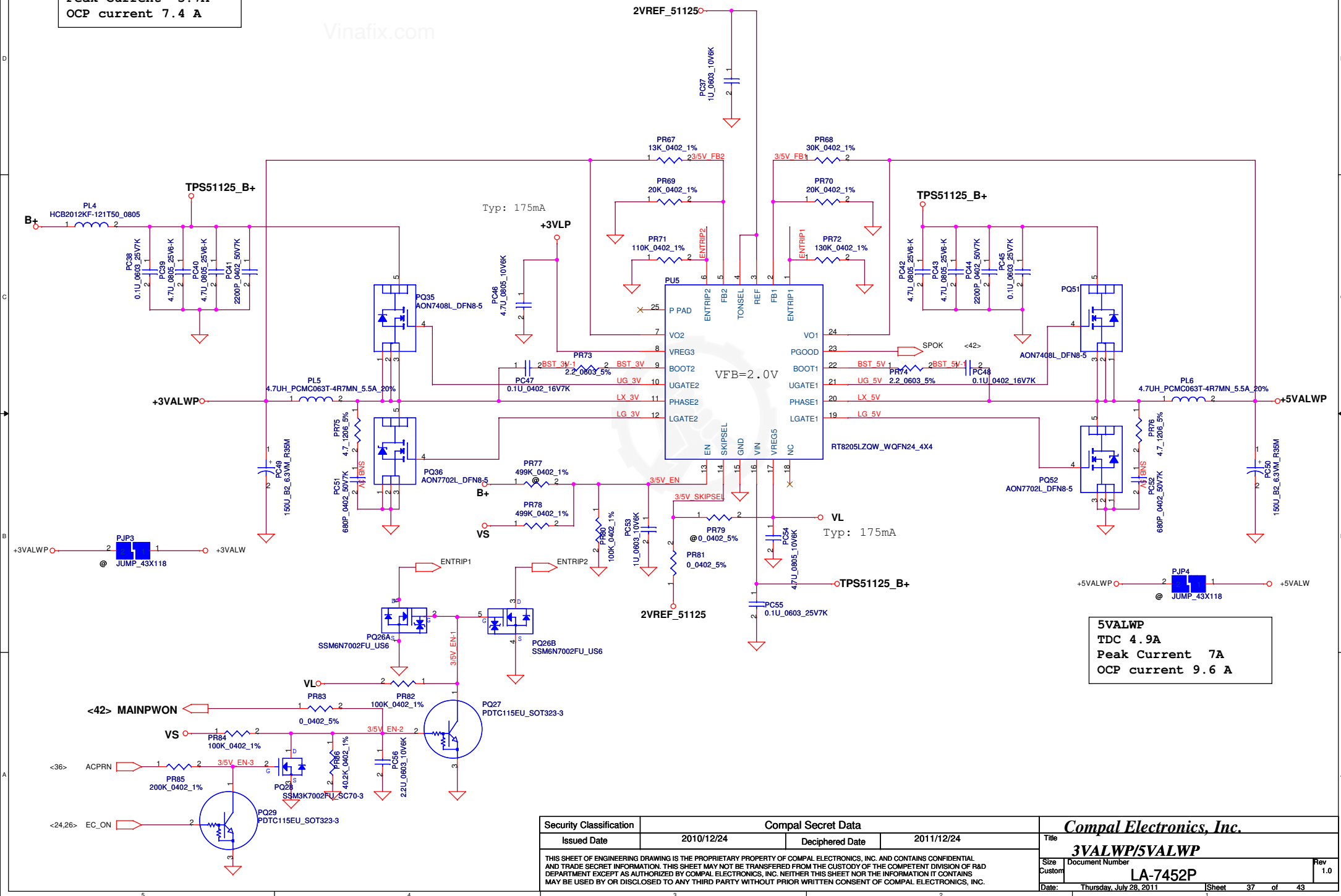
CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

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Issued Date		2010/12/24	Deciphered Date		2011/12/24	Title		
						PWR-CHARGER		
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						Document Number		Rev
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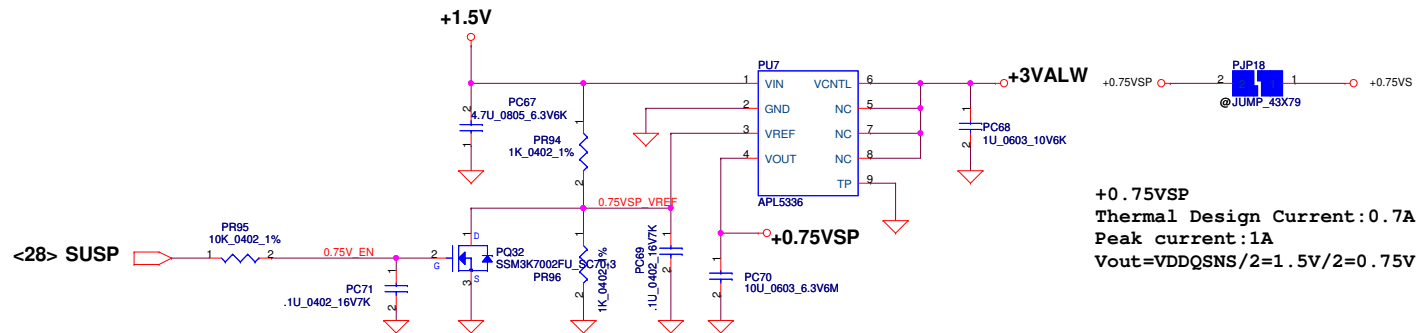
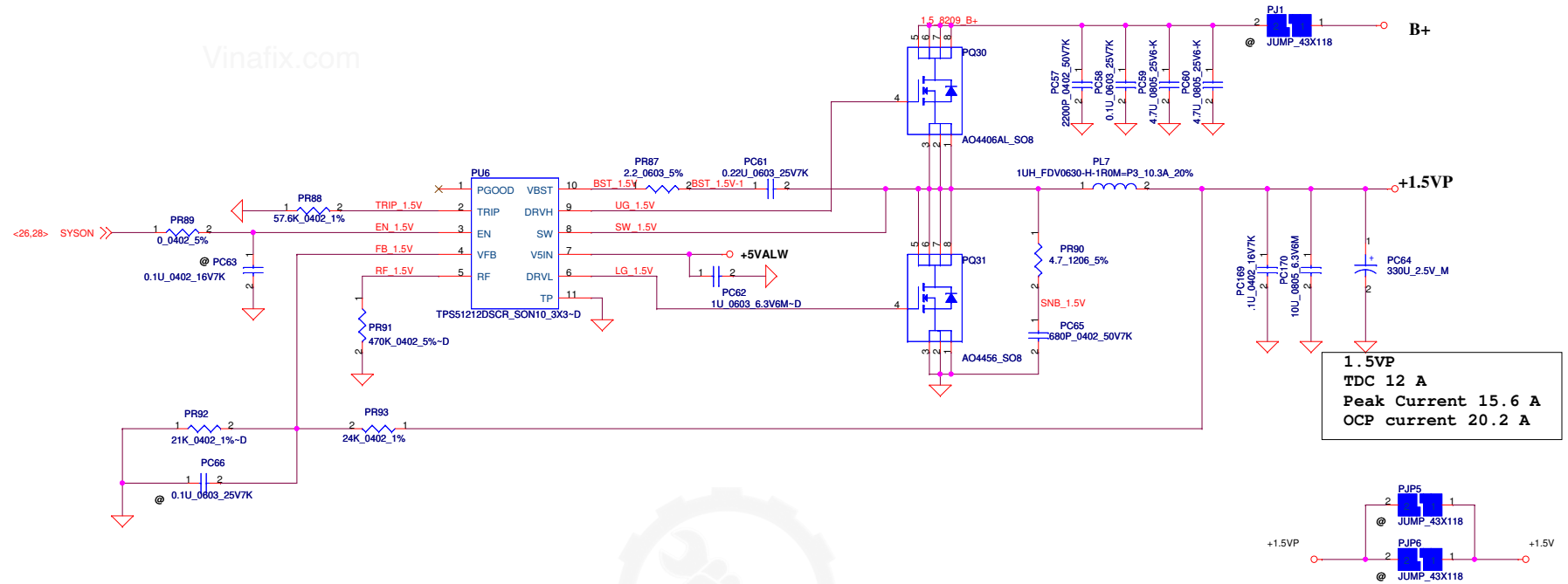
3.3VALWP
TDC 4.02 A
Peak Current 5.7A
OCP current 7.4 A

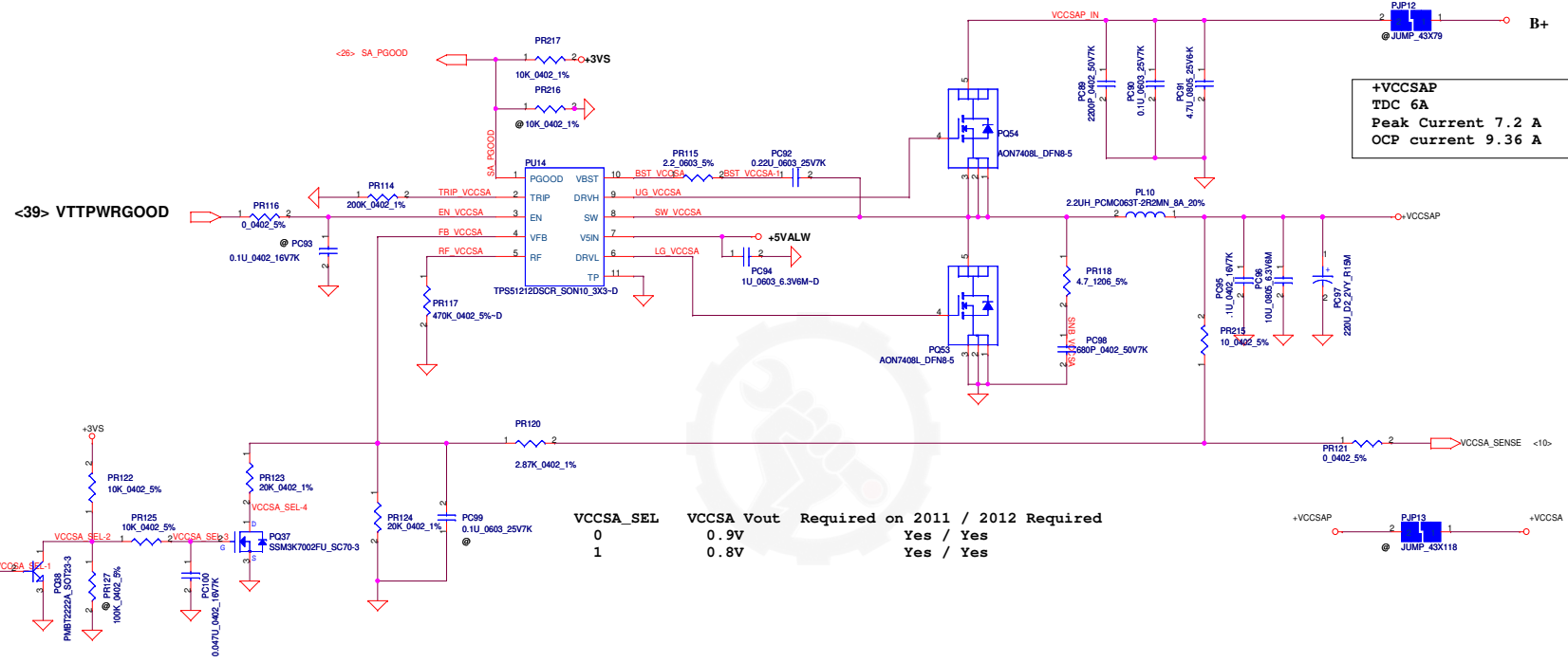
Vinafix.com

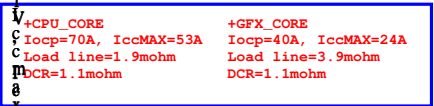


5VALWP
TDC 4.9A
Peak Current 7A
OCP current 9.6 A

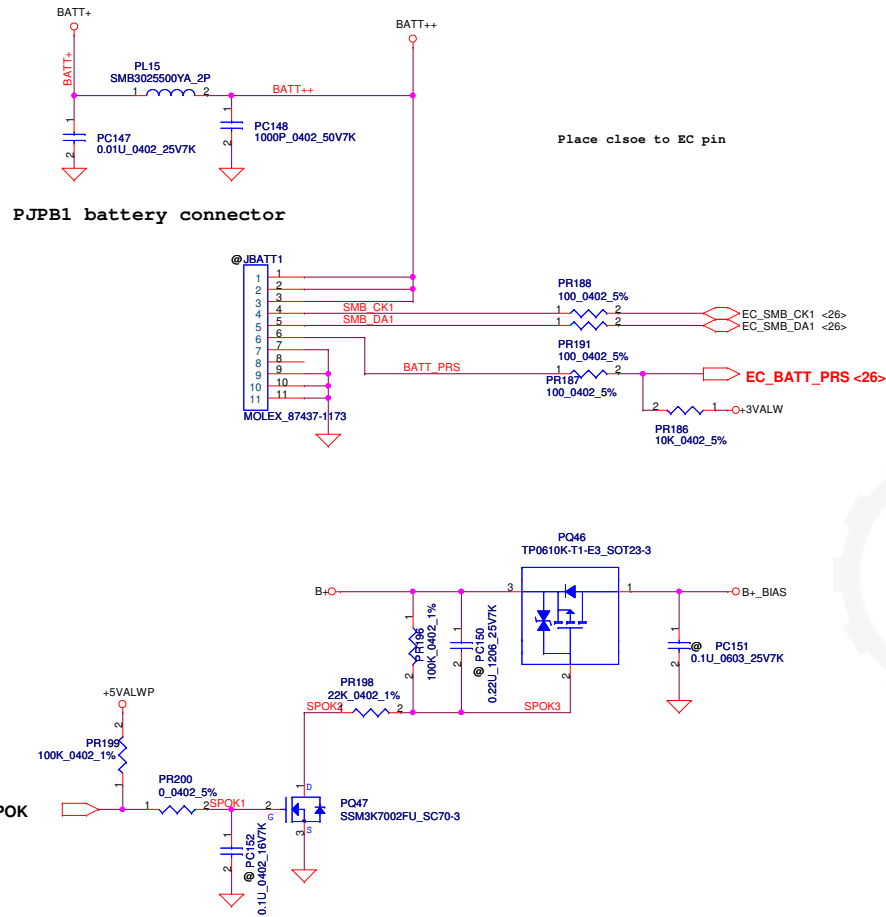
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				Rev	1.0





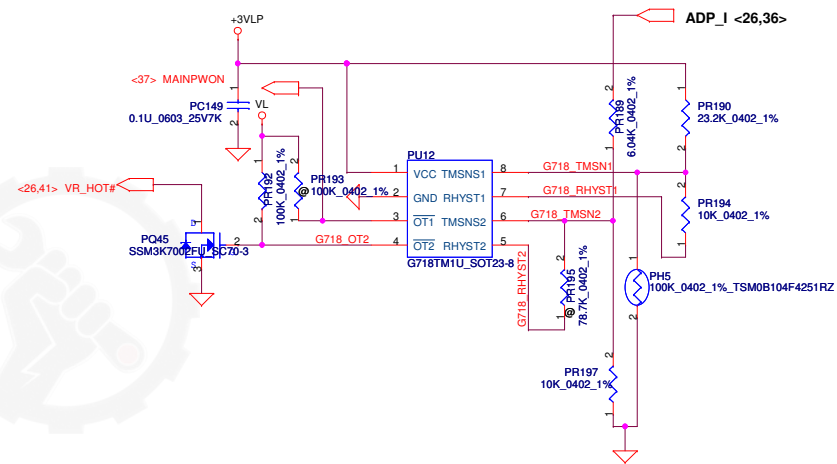


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Title			
CPU_CORE/GFX			
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Battery Connect/OTP

PH3 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C



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Version change list (P.I.R. List)

Page 1 of 1 for PWR

Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	modify Vcore and GFX boost resistance		P46	change PR136,PR163,PR179 to 2.2 +-5% 0603.	2011.2.10	before SSI
2	modify 1.5V Enable signal		P43	change PR81 connect to SYSON.	2011.3.24	SSI
3	integrate mosfet		P45	change PQ53 PQ54 to AON7408L		
4	modify Vcore and GFX's loadline and OCP		P46	change PC137 to .033U 16V K X7R 0402 change PR171 to 1.65K +-1% 0402 change PR149 to 1.33K +-1% 0402 change PR131 to 3.24K +-1% 0402		
5	integrate mosfet		P43	change PQ32 to SSM3K7002FU 1N SC70-3		
			P45	change PQ37 to SSM3K7002FU 1N SC70-3		
6	add capacitance for RF team suggest item		P41	change PC81 PC125 to 10U 25V K X5R 0805 H1.25		
			P43	change PC169 to .1U 16V K X7R 0402		
				change PC170 to 10U 6.3V M X5R 0805 H1.25		
			P44	change PC171 to .1U 16V K X7R 0402		
				change PC172 to 10U 6.3V M X5R 0805 H1.25		
7	modify 1.5V OCP resistance		P43	change PR88 to 57.6K +-1% 0402		
8	modify VCCP OCP resistance		P44	change PR100 to 80.6K +-1% 0402		
9	modify choke footprint for DFX requirement			change PL5,PL6,PL7,PL8,PL10 to TAI-T_VMPI0703AR-100M-Z01_2P		
10	modify PQ11 Vgs resistance		P41	change PR31 to 200K +-1% 0402 change PR35 to 47K +-1% 0402		
11	modify net name SPOK-'		P47	change the net name of PQ47 pin2 to SPOK1 change the net name of PQ47 pin1 to SPOK2 change the net name of PQ46 pin2 to SPOK3		
12	modify PU12 vcc power from +3VALW to +3VLP		P47	change PR190.1 to +3VLP change PR149.1 to +3VLP change PU12.1 to +3VLP		
13	modify OTP resistance		P47	change PR190 to 23.2K +-1% 0402 change PR194 to 10K +-1% 0402		
14	modify VCORE VCCP resistance		P46	change PR145 to 1 +-5% 0603		

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